***EE/CprE/SE 491 WEEKLY REPORT 06***

***March 07, 2022 – March 13, 2022***

***Group number: SDDEC22\_20***

***Project: Implement the i281 CPU in Hardware***

***Client &/Advisor:*** Alexander Stoytchev

***Team Members/Role:***

| **Member** | **Role** |
| --- | --- |
| Alex Kiefer | Project Manager | Lead Hardware Designer |  |
| Saffron Edwards | Software Testing Manager | Website Manager |  |
| David Vachlon | Hardware Testing Manager | Secondary Documenter | Purchasing Manager |
| Patrick O'Brien | Documentation Manager | Meeting Scribe | Secondary Hardware Designer |
| Joseph De Jong | Communications Manager | Secondary Hardware Tester | Secondary Hardware Designer |

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### Individual Contribution

| **NAME**  | **Individual Contributions**  | **Hours this** **week** | **HOURS** **cumulative** |
| --- | --- | --- | --- |
| Alex Kiefer  | Register File, Documentation | 5 | 37 |
| Saffron Edwards | Website, Weekly Reports | 7 | 33 |
| David Vachlon | Ordered Materials, Program Counter | 6 | 34 |
| Patrick O'Brien | EEPROM, Documentation, Progress Report | 5 | 37 |
| Joseph De Jong |  Multiplexors, Data Memory, Group Work, Reports | 6 | 37 |

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### Weekly Summary

*Weekly Objective: Finalize Current i281 Subcomponents*

This week was meant to wrap up current work before spring break. We didn’t want to leave project pieces open-ended. At the end of the week, we completed documentation to store our knowledge.

| **Member** | **Component** |
| --- | --- |
| Alex Kiefer | Register File |
| Saffron Edwards | Website |
| David Vachlon | Program Counter |
| Patrick O'Brien | Multiplexors |
| Joseph De Jong | Multiplexors |

### Progress Report

#### Description of Work Completed:

| **Task Name** | **Members Involved** | **Description** |
| --- | --- | --- |
| Design Schematics for Each Module | All | We developed the high-level schematics for each submodule in the CPU.  |
| Discussion on Instruction Memory and Programmability of the CPU | All | We discussed some of the issues associated with the EEPROM as a memory module in the CPU. We discussed an alternative setup involving a microcontroller and SRAM. This would allow us to read and write to memory while running.  |
| Flags Calculator | Patrick | Designed, assembled and tested the Overflow and Zero Flags. |
| Progress on Register File | Alex | Additional work has gone into the design of the register file. An additional register has been assembled, bringing the total usable registers up to 2.  |
| Program Counter Report | David Vachlon | Documentation and planning on the design of the program counter. |

#### Current Agenda:

| **Task Name** | **Members Involved** | **Due Date** |
| --- | --- | --- |
| Bus Multiplexors | Alex, Joseph, Patrick | March 11 |
| Rebuild Memory File | Joseph | March 4 |
| Rebuild Program Counter | David, Alex | March 4 |
| Complete Register File | Alex | March 11 |
| Build and Test EEPROM Programmer | David, Saffron, Patrick | March 11 |
| Complete ALU | Patrick | March 11 |
| Build Flags Register | Joseph, Patrick | March 11 |
| Opcode Decoder Software and Instruction set | Saffron, David | Spring Break |
| Opcode Decoder Hardware | Alex, Joseph, Patrick | Spring Break |
|  Watch CPU Videos | All | - |
| Learn Altium | All | - |
| Learn KiCad | All | -  |

#### Challenges:

| **Topic** | **Description** |
| --- | --- |
| EEPROM vs SRAM | The current design for the CPU involves the use of EEPROM chips for the instruction and data memory |
| Data Memory | We are unsure of the appropriate approach to implement the data memory. If we were to use an EEPROM or SRAM chip, we would be able to easily read from the data memory but would be unable to view the values stored in each memory address. The online simulation of the i281 CPU shows the data in each memory address, which could be replicated using 8-bit registers for each memory address. This issue will require discussion with the faculty advisor.  |

#### Deliverables:

| **Item** | **Description** |
| --- | --- |
| Flags Calculator Report | [Flags Calculator](https://docs.google.com/document/d/1h2tzEVL_mBArvYDJs527VX9FPO2PzkU5ykD9tnT8W2M/edit?usp=sharing) |
| Programmable Memory Report | [Programmable Memory](https://docs.google.com/document/d/1mYO06MnzUGXRwNfqpNnHAQU9yrBmz-qYzPgde0hQmP0/edit?usp=sharing)  |
| Program Counter Report | [Program Counter](https://docs.google.com/document/d/1BMY4h_pkDqfmcEemdyJwf9zMGCuwKU0NQk9UBZ34RNM/edit?usp=sharing)  |
| High-Level Diagrams Report | [High Level Diagrams](https://docs.google.com/document/d/180hkV42s6hEpT-reSVdn0n7a0LiV-_p3cXmp4mMMduU/edit?usp=sharing) |

### Meeting

#### Attendees:

Alex Kiefer

Saffron Edwards

Patrick O'Brien

David Vachlon

Joseph De Jong

#### To-do:

1. Discuss programmable SRAM with Professor Stoytchev.

#### Notes:

1. Discussed SRAM/ instruction memory
2. Discussed creating a video card for the data memory (display 8 registers)
3. Discussed using KiCad for the schematic/ PCB - Export via Gerber
	1. <http://tuttle.merc.iastate.edu/ee333/topics.htm>
4. Discussed using EEPROM for 7 seg display
	1. 256 X 8 EEPROM
	2. Write a file to program EEPROM
	3. ½ for display
	4. ½ for game mode

#### Action Items:

1. Redesign the programmable memory with an EEPROM
	1. Count how many programs are in the simulator
2. Watch Ben Eater video card videos
3. Try wiring on KiCad
4. Complete Register File
5. Complete Program Count (pending parts)
6. Multiplexors (Mem, ALU, Registers, Flag, PC)
7. Source low-power LEDs
8. Source 8 7-segment indicators