***EE/CprE/SE 491 WEEKLY REPORT 06***

***March 27, 2022 – April 1, 2022***

***Group number: SDDEC22\_20***

***Project: Implement the i281 CPU in Hardware***

***Client &/Advisor:*** [Alexander Stoytchev](mailto:alexs@iastate.edu)

***Team Members/Role:***

| **Member** | **Role** | | |
| --- | --- | --- | --- |
| [Alex Kiefer](mailto:atkiefer@iastate.edu) | Project Manager | Lead Hardware Designer |  |
| [Saffron Edwards](mailto:saffrone@iastate.edu) | Software Testing Manager | Website Manager |  |
| [David Vachlon](mailto:dvachlon@iastate.edu) | Hardware Testing Manager | Secondary Documenter | Purchasing Manager |
| [Patrick O'Brien](mailto:pcobrien@iastate.edu) | Documentation Manager | Meeting Scribe | Secondary Hardware Designer |
| [Joseph De Jong](mailto:jdejong@iastate.edu) | Communications Manager | Secondary Hardware Tester | Secondary Hardware Designer |

***Table Of Contents:***

[Individual Contribution](#_pzsrx86r6sbm) **2**

[Weekly Summary](#_ch1tbostoi65) **2**

[Progress Report](#_dqm8ytk7f9kl) **3**

[Current Agenda](#_2v3c4kpuqd3h) **3**

[Challenges](#_acxa6trzlxbo) **3**

[Attendees](#_lhm2jbzd1g6i) **4**

[Notes](#_arj8tc5n0wxt) **4**

[Action Items](#_40mlfguty7ok) **4**

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### Individual Contribution

| **NAME** | **Individual Contributions** | **Hours this**  **week** | **HOURS**  **cumulative** |
| --- | --- | --- | --- |
| [Alex Kiefer](mailto:atkiefer@iastate.edu) | Register File, Documentation | 8 | 51 |
| [Saffron Edwards](mailto:saffrone@iastate.edu) | Website, Weekly Reports | 5 | 43 |
| [David Vachlon](mailto:dvachlon@iastate.edu) | Ordered Materials, Program Counter | 6 | 46 |
| [Patrick O'Brien](mailto:pcobrien@iastate.edu) | EEPROM, Documentation, Progress Report | 8 | 51 |
| [Joseph De Jong](mailto:jdejong@iastate.edu) | Multiplexores, Data Memory, Group Work, Reports | 8 | 51 |

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### Weekly Summary

*Weekly Objective: Finalize Current i281 Subcomponents*

This week was used to implement the various bus muxes throughout the i281 CPU. We completed 5 Bus Muxes and implemented two. We still need to complete 2 bus muxes and implement 5.

| **Member** | **Component** |
| --- | --- |
| [Alex Kiefer](mailto:atkiefer@iastate.edu) | Bus Mux |
| [Saffron Edwards](mailto:saffrone@iastate.edu) | Bus Mux |
| [David Vachlon](mailto:dvachlon@iastate.edu) | Bus Mux |
| [Patrick O'Brien](mailto:pcobrien@iastate.edu) | Bus Mux |
| [Joseph De Jong](mailto:jdejong@iastate.edu) | Bus Mux |

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### Progress Report

| **Task Name** | **Members Involved** | **Description** |
| --- | --- | --- |
| Finished ALU with Bus Muxs | Patrick O’Brien | Implemented all ALU operations needed |
| Work on Register File | Alex Kiefer | Finished half of the 4 to 1 bus mux |
| Work on Bus Multiplexores | Joe De Jong, David Vachlon | Work started on the 8-bit bus multiplexer. |
| Parts Orders | David Vachlon and Patrick O’Brien | 50W power supply as well as more low power LED’s |

### Current Agenda

| **Task Name** | **Members Involved** | **Due Date** |
| --- | --- | --- |
| Bus Multiplexores | Alex, Joseph, Patrick | March 11 |
| Rebuild Memory File | Joseph | March 4 |
| Rebuild Program Counter | David, Alex | March 4 |
| Complete Register File | Alex | March 11 |
| Build and Test EEPROM Programmer | David, Saffron, Patrick | March 11 |
| Complete ALU | Patrick | March 11 |
| Build Flags Register | Joseph, Patrick | March 11 |
| Opcode Decoder Software and Instruction set | Saffron, David | Spring Break |
| Opcode Decoder Hardware | Alex, Joseph, Patrick | Spring Break |
| Learn KiCad | All | - |

### Challenges

| **Topic** | **Description** |
| --- | --- |
| EEPROM vs SRAM | The current design for the CPU involves the use of EEPROM chips for the instruction and data memory |
| Data Memory | We are unsure of the appropriate approach to implementing the data memory. If we were to use an EEPROM or SRAM chip, we would be able to easily read from the data memory but would be unable to view the values stored in each memory address. The online simulation of the i281 CPU shows the data in each memory address, which could be replicated using 8-bit registers for each memory address. This issue will require discussion with the faculty advisor. |

491 Friday Meeting

Meeting Notes 04/01

horizontal line

### Attendees

[Alex Kiefer](mailto:atkiefer@iastate.edu)

[Saffron Edwards](mailto:saffrone@iastate.edu)

[Patrick O'Brien](mailto:pcobrien@iastate.edu)

[David Vachlon](mailto:dvachlon@iastate.edu)

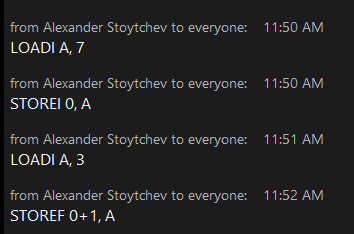
[Joseph De Jong](mailto:jdejong@iastate.edu)

### Notes

1. Talked to Dr. Duwe about programming
   1. Recommended making our own assembler
   2. Utilize a PI to program the CPU
      1. PI will require 3 computers- Excess steps
2. Discussed Compiler
   1. Written in java on the class page
   2. <https://www.ece.iastate.edu/~alexs/classes/2021_Fall_281/i281_CPU/>
3. Fix

### Action Items

1. Ask ETG about PCB printing
   1. With the option of the company solders
2. Brainstorm how to reset the board without reprogramming
3. Schedule a meeting with Dr. Duwe
4. Find wood or plastic backplate
   1. Plastic: Not white
5. Finish 4-bit Flag Register
6. Finish Register output MUX
7. Find EEPROM for Instruction Memory and program it
   1. Learn EEPROM and write to chip
8. Write to Data Memory at the start of execution until we find a new Data Memory option



1. Memmory Mapped I/O
2. Video Cards
3. 8-bit register chip

**EE491 Senior Design**

**i281 CPU Project**

**Joseph De Jong**

**2t1\_8B Mux Module**

**Introduction:**

This week our team focused on creating 2t1\_8B muxes. These muxes will be utilized in 4 separate locations on the i281 CPU. An additional 6-bit mux will be used in the program counter.

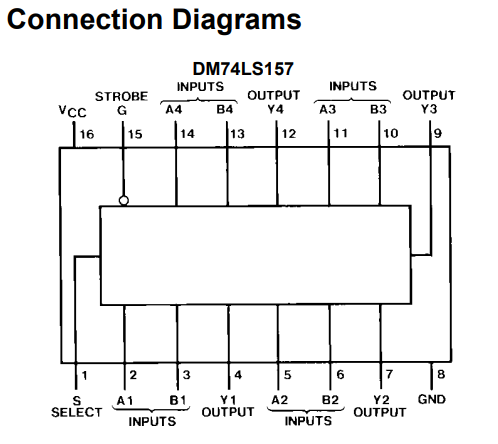
**Parts List:**

| **Part Name** | **Quantity** | **Description** |
| --- | --- | --- |
| 74LS157 Quad 2-Line to 1-Line Data Selectors | 10 (2 per mux) | Array of 4, 1-bit muxes |
| 22awg solid core wire | 5ft | Wire for interconnections |
| Breadboard | 5 |  |

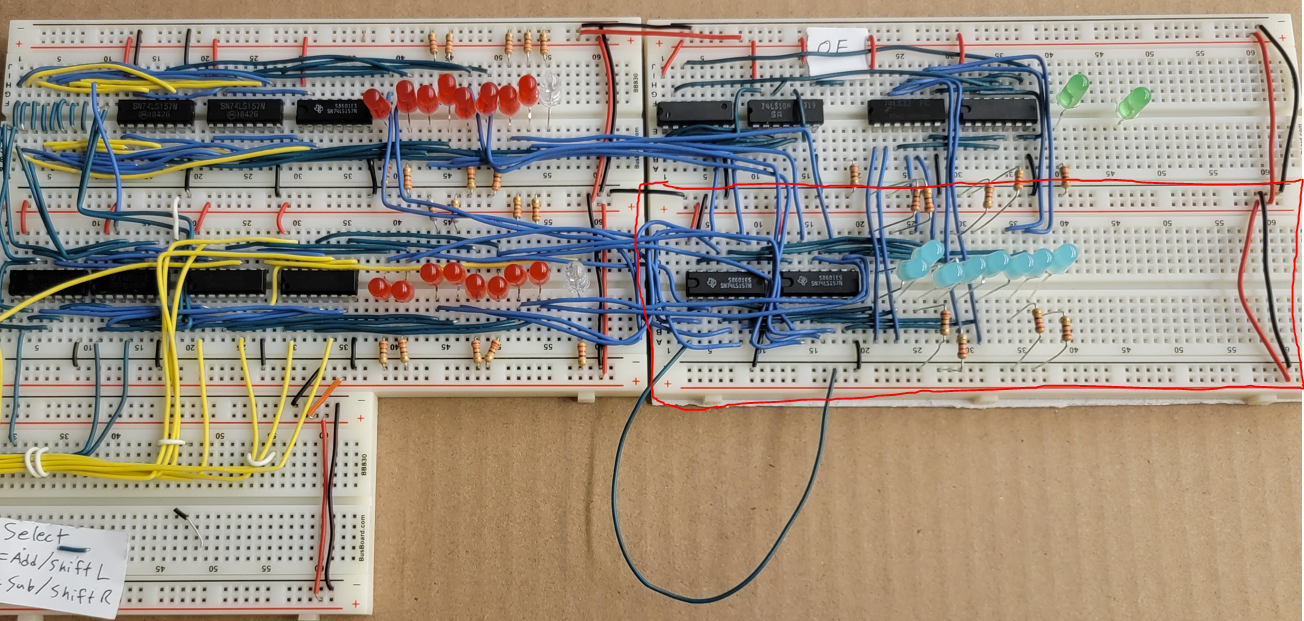
**Assembly:**

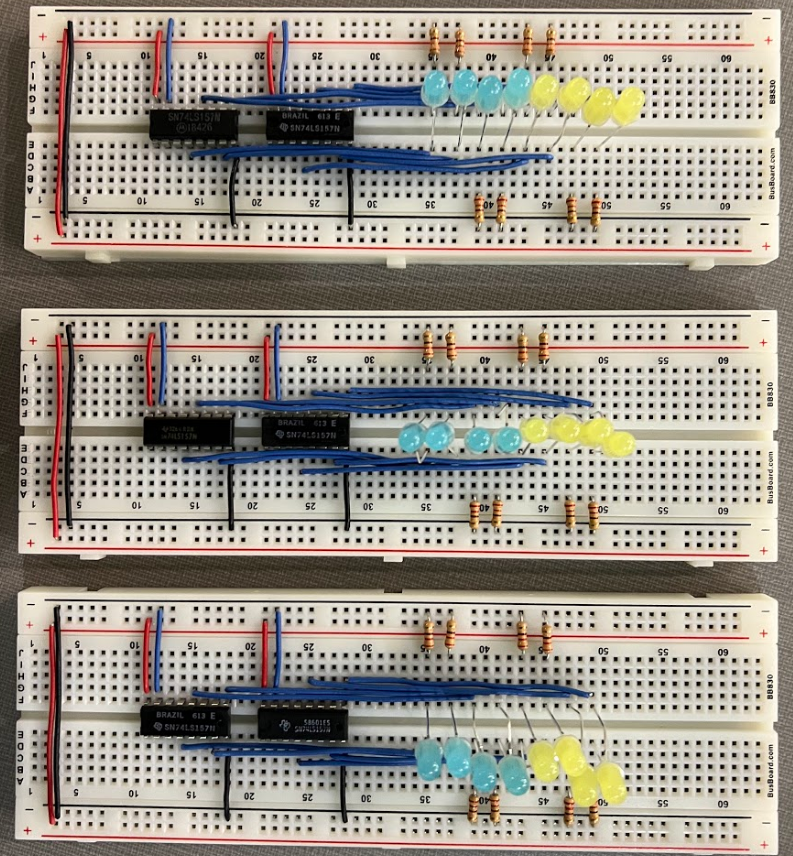
**Schematic**

This schematic was taken from the [datasheet](https://www.jameco.com/Jameco/Products/ProdDS/46771.pdf) for the 74LS157 chipset. The entire chip is controlled by a strobe pin (also known as an enable) and a select pin. Each chip has 4, 1-bit muxes. To create an 8-bit mux we will utilize two chips per device.

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**Assembled MUXES:**

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Blue Wires: Data Wires

Enable Bit

Mux Output to LEDs

Red Wires: +5V

Black Wire: GND