***EE/CprE/SE 491 WEEKLY REPORT 06***

***April 04, 2022 – April 08, 2022***

***Group number: SDDEC22\_20***

***Project: Implement the i281 CPU in Hardware***

***Client &/Advisor:*** [Alexander Stoytchev](mailto:alexs@iastate.edu)

***Team Members/Role:***

| **Member** | **Role** | | |
| --- | --- | --- | --- |
| [Alex Kiefer](mailto:atkiefer@iastate.edu) | Project Manager | Lead Hardware Designer |  |
| [Saffron Edwards](mailto:saffrone@iastate.edu) | Software Testing Manager | Website Manager |  |
| [David Vachlon](mailto:dvachlon@iastate.edu) | Hardware Testing Manager | Secondary Documenter | Purchasing Manager |
| [Patrick O'Brien](mailto:pcobrien@iastate.edu) | Documentation Manager | Meeting Scribe | Secondary Hardware Designer |
| [Joseph De Jong](mailto:jdejong@iastate.edu) | Communications Manager | Secondary Hardware Tester | Secondary Hardware Designer |

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### Individual Contribution

| **NAME** | **Individual Contributions** | **Hours this**  **week** | **HOURS**  **cumulative** |
| --- | --- | --- | --- |
| [Alex Kiefer](mailto:atkiefer@iastate.edu) | Register File | 6 | 57 |
| [Saffron Edwards](mailto:saffrone@iastate.edu) | Compiler/ Assembler, Decoder | 5 | 48 |
| [David Vachlon](mailto:dvachlon@iastate.edu) | Ordered Materials, Program Counter | 7 | 53 |
| [Patrick O'Brien](mailto:pcobrien@iastate.edu) | Documentation, Flag Register | 6 | 57 |
| [Joseph De Jong](mailto:jdejong@iastate.edu) | Documentation, Bus Muxes | 6 | 57 |

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### Weekly Summary

#### Weekly Objective:

Finalize Current i281 Subcomponents

This week caused many roadblocks. We have run into issues implementing the final subcomponents of the i281 CPU. This is due to the implementation of hardware over software. We will be brainstorming new ways to avoid the issues of filling memory before execution.

| **Member** | **Component** |
| --- | --- |
| [Alex Kiefer](mailto:atkiefer@iastate.edu) | Register File |
| [Saffron Edwards](mailto:saffrone@iastate.edu) | Compiler |
| [David Vachlon](mailto:dvachlon@iastate.edu) | Program Counter |
| [Patrick O'Brien](mailto:pcobrien@iastate.edu) | Bus Mux |
| [Joseph De Jong](mailto:jdejong@iastate.edu) | Bus Mux |

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### Progress Report

| **Task Name** | **Members Involved** | **Description** |
| --- | --- | --- |
| Finished ALU with Bus Muxs | Patrick O’Brien | Implemented all ALU operations needed |
| Work on Register File | Alex Kiefer | Finished half of the 4 to 1 bus mux |
| Work on Bus Multiplexores | Joe De Jong, David Vachlon | Work started on the 8-bit bus multiplexer. |
| Parts Orders | David Vachlon and Patrick O’Brien | Ordered Decoders and Test Registers |

### Current Agenda

| **Task Name** | **Members Involved** | **Due Date** |
| --- | --- | --- |
| Bus Multiplexores | Alex, Joseph, Patrick | March 11 |
| Rebuild Memory File | Joseph | March 4 |
| Rebuild Program Counter | David, Alex | March 4 |
| Complete Register File | Alex | March 11 |
| Build and Test EEPROM Programmer | David, Saffron, Patrick | March 11 |
| Complete ALU | Patrick | March 11 |
| Build Flags Register | Joseph, Patrick | March 11 |
| Opcode Decoder Software and Instruction set | Saffron, David | Spring Break |
| Opcode Decoder Hardware | Alex, Joseph, Patrick | Spring Break |
| Learn KiCad | All | - |

### Challenges

| **Topic** | **Description** |
| --- | --- |
| EEPROM vs SRAM | The current design for the CPU involves the use of EEPROM chips for the instruction and data memory |
| Data Memory | We are unsure of the appropriate approach to implementing the data memory. If we were to use an EEPROM or SRAM chip, we would be able to easily read from the data memory but would be unable to view the values stored in each memory address. The online simulation of the i281 CPU shows the data in each memory address, which could be replicated using 8-bit registers for each memory address. This issue will require discussion with the faculty advisor. |
| OpCode | The current i281 CPU utilizes every possible OpCode. This doesn’t leave the team the ability to add a possible instruction to fill data memory before execution. Our team will be brainstorming ways to implement new OpCodes. |

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### Meeting Notes 04/01

#### Attendees

[Alex Kiefer](mailto:atkiefer@iastate.edu)

[Saffron Edwards](mailto:saffrone@iastate.edu)

[Patrick O'Brien](mailto:pcobrien@iastate.edu)

[David Vachlon](mailto:dvachlon@iastate.edu)

[Joseph De Jong](mailto:jdejong@iastate.edu)

#### Notes

1. Discussed Possible Memory Devices
   1. Implement DMEM as register file
2. How to handle filling DMEM during startup
3. Possible IMEM storage devices
   1. New OPCODES and datapaths for DMEM filling

#### Next Week's Objectives:

1. Finish Current Devices
   1. Alex: Reg File
   2. Joe: Bus Muxes
   3. David: Program Counter
   4. Patrick: Flag Registers
   5. Saffron: Assembler/ Compiler
2. Find Possible DMEM registers
   1. 74 LS Series Preferred
3. Record Currently Used Parts